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EXAMINER	
O BRIEN, BARRY J	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/22/2004 7

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/751,372	JARVIS ET AL.
	Examiner	Art Unit
	Barry J. O'Brien	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Amendment A as received on 2/24/2004.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greenley, U.S. Patent No. 5,761,469, in view of Dye, U.S. Patent No. 6,412,061.

7. Regarding claims 1 and 14, taking claim 14 as exemplary, Greenley has taught a processing system comprising:

a. A data processor (100 of Fig.1).

b. A memory coupled to said data processor (see Col.1 lines 41-43).

c. Wherein said data processor comprises:

i. An instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline (see Col.1 lines 34-40).

ii. A data cache (180 of Fig.1) capable of storing data values used by said pending instruction (see Col.1 lines 42-43).

iii. A plurality of registers (150 of Fig.1) capable of receiving said data values from said data cache (see Col.1 lines 41-45).

iv. A load store unit (130 of Fig.1) capable of transferring a first one of said data values from said data cache to a target one of said plurality of registers during execution of a load operation (see Col.1 lines 15-21, 63-67 and Col.2 lines 1-7, 13-15).

v. A shifter circuit (160,170 of Fig.1) associated with said load store unit capable of one of a) shifting (see Col.2 lines 19-31), b) sign extending (see Col.2 lines 48-54), and c) zero extending (see Col.2 lines 45-47) said first data value prior to loading said first data value into said target register.

8. Greenley has not explicitly taught bypass circuitry associated with said load store unit capable of transferring said first data value from said data cache directly to said target register without processing said first data value in said shifter circuit.

9. However, Dye has taught the bypassing of portions of a circuit that are not needed in order to reduce the latency inherent with such circuitry as instructions are executed (see Abstract and Col.3 lines 2-11, 35-43). Greenley has taught a sign extension unit (160 of Fig.1) that fills in unoccupied bits of a register by extending its sign after it is loaded from the data cache (see Col.2 lines 48-50). This implies that when fetched data occupies the entire register no sign extension is necessary because there are no unoccupied bits, thereby making the sign extension and alignment units unnecessary in certain circumstances. Therefore, one of ordinary skill in the art would have found it obvious to modify Greenley to include a bypass path around the unused sign extension and aligning units because doing so would reduce the latency required to load data (see Dye Col.3 lines 2-11 and 35-43).

10. Greenley has also not explicitly taught the processing system comprising a plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor.

11. However, Dye has taught the inclusion of a graphics coprocessor and a memory mapped frame buffer connected to the processor via system bus which perform specific tasks in order to free up the main processor to perform other general operations (see Col.2 lines 21-35). Therefore, one of ordinary skill in the art would have found it obvious to include a graphics coprocessor and frame buffer as a memory-mapped peripheral circuit in the processor of

Greenley in order to allow the main processor to perform general tasks in order to free up processor cycles (see Dye, Col.2 lines 21-25).

12. Claim 1 is nearly identical to claim 14. Claim 1 differs in its lack of a main memory and memory-mapped peripheral circuits, but comprises the same data processor as claim 14, and is therefore rejected for the same reasons.

13. Regarding claims 2 and 15, taking claim 15 as exemplary, Greenley in view of Dye has taught the processing system as set forth in claim 1, wherein said bypass circuitry transfers said first data value from said data cache directly to said target register during a load word operation (see above rejection of claim 1, as well as Dye Col.3 lines 2-11 and 35-43). While Greenley has taught a different register size than the applicant (see Col.2 lines 17-19), the situation when a register has no unoccupied bits after being loaded with data from a data cache remains the same, with the size of the register and word being moot. Therefore Greenley's loading of a double word has the same consequences as the applicant's loading of a word.

14. Claim 2 is nearly identical to claim 15. Claim 2 differs in its parent claim, but comprises the same data processor as claim 15, and is therefore rejected for the same reasons.

15. Regarding claims 3 and 16, taking claim 16 as exemplary, Greenley in view of Dye has taught the data processor as set forth in claim 2, wherein said bypass circuitry transfers said first data value from said data cache directly to said target register at the end of two machine cycles (see Col.4 lines 17-20). However, Greenley has taught this two-cycle latency for all load instructions, including those without the need for sign extension. In the situation where the load instruction fills the target register completely and no sign extension is needed, such as during the applicant's load word or Greenley's load double word, the data processor as configured above

will execute the load instruction one cycle faster (see Dye Col.3 lines 2-11, 35-43). This will create a latency of one cycle for those load instructions which bypass the sign extension unit, and two cycles for those which need sign extension. Because the applicant's claimed load instructions, which take 2 and 3 cycles for bypassed and sign-extended instructions, respectively, have no claimed advantages over the 1 and 2 cycles that Greenly in view of Dye have taught, but are merely a change in the magnitude of latency, they are considered to be equivalent and thus taught by Greenley in view of Dye (see *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

16. Claim 3 is nearly identical to claim 16. Claim 3 differs in its parent claim, but comprises the same data processor as claim 16, and is therefore rejected for the same reasons.

17. Regarding claims 4 and 17, taking claim 17 as exemplary, Greenley in view of Dye has taught the data processor as set forth in claim 1, wherein said shifter circuit one of a) shifts, b) sign extends, or c) zero extends said first data value prior to loading said first data value into said target register during a load half-word operation (see Greenley Col.2 lines 17-20, 24-30, 46-47).

18. Claim 4 is nearly identical to claim 17. Claim 4 differs in its parent claim, but comprises the same data processor as claim 17, and is therefore rejected for the same reasons.

19. Regarding claims 5 and 18, taking claim 18 as exemplary, Greenley in view of Dye has taught the data processor as set forth in claim 4, wherein said shifter circuit loads said shifted first data value into said target register at the end of two machine cycles (see Col.4 lines 17-20), but has not explicitly taught the load taking three machine cycles. However, Greenley has taught this two-cycle latency for all load instructions, including those without the need for sign extension. In the situation where the load instruction fills the target register completely and no

sign extension is needed, such as during the applicant's load word or Greenley's load double word, the data processor as configured above will execute the load instruction one cycle faster (see Dye Col.3 lines 2-11, 35-43). This will create a latency of one cycle for those load instructions which bypass the sign extension unit, and two cycles for those which need sign extension, such as half-word load instructions. Because the applicant's claimed load instructions, which take 2 and 3 cycles for bypassed and sign-extended instructions, respectively, have no claimed advantages over the 1 and 2 cycles that Greenly in view of Dye have taught, but are merely a change in the magnitude of latency, they are considered to be equivalent and thus taught by Greenley in view of Dye (see *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

20. Claim 5 is nearly identical to claim 18. Claim 5 differs in its parent claim, but comprises the same data processor as claim 18, and is therefore rejected for the same reasons.

21. Regarding claims 6 and 19, taking claim 19 as exemplary, Greenley in view of Dye has taught the data processor as set forth in claim 1, wherein said shifter circuit one of a) shifts, b) sign extends, and c) zero extends said first data value prior to loading said first data value into said target register during a load byte operation (see Greenley Col.2 lines 17-20, 36-40, 46-47).

22. Claim 6 is nearly identical to claim 19. Claim 6 differs in its parent claim, but comprises the same data processor as claim 19, and is therefore rejected for the same reasons.

23. Regarding claims 7 and 20, taking claim 20 as exemplary, Greenley in view of Dye has taught the data processor as set forth in claim 6, wherein said shifter circuit loads said shifted first data value into said target register at the end of two machine cycles (see Col.4 lines 17-20), but has not explicitly taught the load taking three machine cycles. However, Greenley has taught

this two-cycle latency for all load instructions, including those without the need for sign extension. In the situation where the load instruction fills the target register completely and no sign extension is needed, such as during the applicant's load word or Greenley's load double word, the data processor as configured above will execute the load instruction one cycle faster (see Dye Col.3 lines 2-11, 35-43). This will create a latency of one cycle for those load instructions which bypass the sign extension unit, and two cycles for those which need sign extension, such as byte load instructions. Because the applicant's claimed load instructions, which take 2 and 3 cycles for bypassed and sign-extended instructions, respectively, have no claimed advantages over the 1 and 2 cycles that Greenley in view of Dye have taught, but are merely a change in the magnitude of latency, they are considered to be equivalent and thus taught by Greenley in view of Dye (see *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

24. Claim 7 is nearly identical to claim 20. Claim 7 differs in its parent claim, but comprises the same data processor as claim 20, and is therefore rejected for the same reasons.

25. Regarding claims 8 and 21, taking claim 21 as exemplary, Greenley in view of Dye has taught the data processor as set forth in claim 1, but has not explicitly taught wherein said bypass circuitry comprises a multiplexer having a first input channel coupled to a data output of said data cache.

26. However, Dye has taught the multiplexer (322 of Fig.3) selecting between data from the current stage and data that has been bypassed from the prior stage (see Fig.3 and Col.9 lines 41-55). As taught above in the rejection of claim 1, Greenley in view of Dye has taught the use of a bypass circuit around the sign extension and alignment units when certain types of load

instructions are executed. Because not all load instructions are to use the bypass, such as load byte and load half-word instructions, the circuit must have the ability to select between using the bypass circuit or not. Therefore, one of ordinary skill in the art would have found it obvious to use the multiplexer (Dye, 322 of Fig.3) to select between data coming from the data cache and the sign extension/alignment units so that the latter units are not always bypassed so the correct datapath is chosen.

27. Claim 8 is nearly identical to claim 21. Claim 8 differs in its parent claim, but comprises the same data processor as claim 21, and is therefore rejected for the same reasons.

28. Regarding claims 9 and 22, taking claim 22 as exemplary, Greenley in view of Dye has taught the data processor as set forth in claim 8, wherein said multiplexer (Dye, 322 of Fig.3) has a second input channel coupled to an output of said shifter circuit. As taught above in the rejection of claim 8, the multiplexer (Dye, 322 of Fig.3) selects between the output of the data cache and the sign extension/alignment units so that the correct datapath is chosen.

29. Claim 9 is nearly identical to claim 22. Claim 9 differs in its parent claim, but comprises the same data processor as claim 22, and is therefore rejected for the same reasons.

30. Regarding claim 10, Greenley has taught for use in a processor comprising an N-stage execution pipeline (see Col.1 lines 34-40), a data cache (180 of Fig.1), and a plurality of registers (150 of Fig.1), a method of loading a first data value from the data cache into a target one of the registers, the method comprising the steps of:

a. Determining if a pending instruction in the execution pipeline is one of a load word operation, a load half-word operation, and a load byte operation (see Col.1 lines 63-67, Col.2 lines 1-7, 17-19 and Col.5 lines 13-24).

b. In response to a determination that the pending instruction is a load half-word operation, transferring the first data value from the data cache to a shifter circuit and shifting the first data value prior to loading the first data value into the target register (see Col.2 lines 24-31).

c. In response to a determination that the pending instruction is a load byte operation, transferring the first data value from the data cache to a shifter circuit and shifting the first data value prior to loading the first data value into the target register (see Col.2 lines 35-40).

31. Greenley has not explicitly taught where in response to a determination that the pending instruction is a load word operation, transferring the first data value from the data cache directly to the target register without processing the first data value in the shifter circuit.

32. However, Dye has taught the bypassing of portions of a circuit that are not needed in order to reduce the latency inherent with such circuitry as instructions are executed (see Abstract and Col.3 lines 2-11, 35-43). Greenley has taught a sign extension unit (160 of Fig.1) that fills in unoccupied bits of a register by extending its sign after it is loaded from the data cache (see Col.2 lines 48-50). This implies that when fetched data occupies the entire register no sign extension is necessary because there are no unoccupied bits, thereby making the sign extension and alignment units unnecessary in certain circumstances. Therefore, one of ordinary skill in the art would have found it obvious to modify Greenley to include a bypass path around the unused sign extension and aligning units because doing so would reduce the latency required to load data (see Dye Col.3 lines 2-11 and 35-43).

33. Regarding claim 11, Greenley in view of Dye has taught the method as set forth in claim 10, wherein the step of transferring the first data value requires two machine cycles during a load word operation (see Col.4 lines 17-20). However, Greenley has taught this two-cycle latency for all load instructions, including those without the need for sign extension. In the situation where the load instruction fills the target register completely and no sign extension is needed, such as during the applicant's load word or Greenley's load double word, the data processor as configured above will execute the load instruction one cycle faster (see Dye Col.3 lines 2-11, 35-43). This will create a latency of one cycle for those load instructions which bypass the sign extension unit, and two cycles for those which need sign extension. While Greenley has taught a different register size than the applicant (see Col.2 lines 17-19), the situation when a register has no unoccupied bits after being loaded with data from a data cache remains the same, with the size of the register and word being moot. Therefore Greenley's loading of a double word has the same consequences as the applicant's loading of a word. Because the applicant's claimed load instructions, which take 2 and 3 cycles for bypassed and sign-extended instructions, respectively, have no claimed advantages over the 1 and 2 cycles that Greenley in view of Dye have taught, but are merely a change in the magnitude of latency, they are considered to be equivalent and thus taught by Greenley in view of Dye (see *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

34. Regarding claim 12, Greenley in view of Dye has taught the method as set forth in claim 10, wherein the step of transferring the first data value requires two machine cycles during a load half-word operation (see Col.4 lines 17-20), but has not explicitly taught the transfer taking three machine cycles. However, Greenley has taught this two-cycle latency for all load instructions,

including those without the need for sign extension. In the situation where the load instruction fills the target register completely and no sign extension is needed, such as during the applicant's load word or Greenley's load double word, the data processor as configured above will execute the load instruction one cycle faster (see Dye Col.3 lines 2-11, 35-43). This will create a latency of one cycle for those load instructions which bypass the sign extension unit, and two cycles for those which need sign extension, such as half-word load instructions. Because the applicant's claimed load instructions, which take 2 and 3 cycles for bypassed and sign-extended instructions, respectively, have no claimed advantages over the 1 and 2 cycles that Greenly in view of Dye have taught, but are merely a change in the magnitude of latency, they are considered to be equivalent and thus taught by Greenley in view of Dye (see *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

35. Regarding claim 13, Greenley in view of Dye has taught the method as set forth in claim 10 wherein the step of transferring the first data value requires two machine cycles during a load byte operation (see Col.4 lines 17-20), but has not explicitly taught the transfer taking three machine cycles. However, Greenley has taught this two-cycle latency for all load instructions, including those without the need for sign extension. In the situation where the load instruction fills the target register completely and no sign extension is needed, such as during the applicant's load word or Greenley's load double word, the data processor as configured above will execute the load instruction one cycle faster (see Dye Col.3 lines 2-11, 35-43). This will create a latency of one cycle for those load instructions which bypass the sign extension unit, and two cycles for those which need sign extension, such as half-word load instructions. Because the applicant's claimed load instructions, which take 2 and 3 cycles for bypassed and sign-extended instructions,

respectively, have no claimed advantages over the 1 and 2 cycles that Greenly in view of Dye have taught, but are merely a change in the magnitude of latency, they are considered to be equivalent and thus taught by Greenley in view of Dye (see *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

Response to Arguments

36. Applicant's arguments filed 2/24/2004 have been fully considered but they are not persuasive.

37. On page 14, paragraph 1, of the present amendment, the Applicant argues, in essence:

"*...the aligning unit of Greenley cannot be skipped when data having 64 bits is retrieved as asserted in the Office Action. Instead, the aligning unit must examine the contents of the retrieved data to ensure that it is properly aligned. Similarly, Greenley specifically recites that the sign extension unit operates on retrieved data even when a double word (64 bits) is received from the aligning unit. Based on this, the sign extension unit of Greenley cannot be skipped when data having 64 bits is retrieved as asserted in the Office Action. As a result, Greenley cannot be modified to transfer a "first data value" from a "data cache" directly to a "target register" without processing the first data value in a "shifter circuit" as recited in claims 1, 10 and 14*".

38. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See below paragraph 44 for an explanation of the motivation of the

combination Greenley in view of Dye. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

39. On page 14, paragraph 2, of the present amendment, the Applicant further argues, in essence:

> *"Moreover, Dye recites a method for adjusting a processor pipeline and bypassing unnecessary stages. In other words, Dye simply recites skipping stages of a pipeline. Dye contains no mention of bypassing a "shifter circuit" that is separate from an "execution pipeline" as recited in claims 1, 10 and 14".*

40. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See below paragraph 44 for explanation of the motivation for the combination of Greenley in view of Dye. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

41. Furthermore, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a shifter circuit that is <u>separate</u> from an execution pipeline) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

42. On page 14, paragraph 3, of the present amendment, the Applicant further argues, in essence:

"For these reasons, there is no motivation to modify Greenley so as to bypass the aligning unit and the sign extension unit. In particular, there is no motivation to modify Greenley using "bypass circuitry" capable of transferring a "first data value" from a "data cache" directly to a "target register" without processing the first data value in a "shifter circuit" as recited in Claims 1 and 14. Also, there is no motivation to modify Greenley so as to transfer a "first data value" from a "data cache" directly to a "target register" without processing the first data value in a "shifter circuit" as recited in claim 10."

43. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988), and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

44. Here, Greenley simply shows a datapath that can transfer a "first data value" from a "data cache" to a "target register" via the sign extension and aligning units (see Fig.1 of Greenley, as well as above paragraphs 7-12). While Greenley has not explicitly taught the bypassing of the sign extension unit (as shown in paragraph 8 above), that does not mean it cannot be skipped as part of a theoretical combination as the Applicant states. The motivation to modify the datapath to bypass the sign extension unit does not come from Greenley as the Applicant argues. Instead, it comes from the Dye reference, which has taught bypassing portions of a circuit that are not

needed in order to reduce the latency inherent in such circuitry (see Abstract and Col.3 lines 2-11, 35-43 of Dye). When data is fetched that occupies the entire register, no sign extension is necessary because of the lack of unoccupied bits, and thus sign extension and alignment units circuitry becomes unnecessary under these circumstances (see above paragraph 9). For example, Patterson et al., *Computer Organization & Design: The Hardware/Software Interface* has taught that attempting to sign extend a 32-bit word loaded into a 32-bit register is a moot operation as no unoccupied bits are available to sign extend (see p.214 of Patterson). Therefore, as was cited in the previous office action (see paragraphs 10-15 of the office action dated 11/18/03), and again in paragraphs 7-12 above, one of ordinary skill in the art would have found it obvious to modify a processor to bypass circuitry that performs a moot operation so that latency in executing instructions that would have used said circuitry is reduced.

45. On page 15, paragraph 2, of the present amendment, the Applicant further argues, in essence:

> *"Dye contains no mention of transferring a data value to different locations based on whether a pending instruction is a load half-word operation, a load-byte operation, or a load-word operation. Greenley simply recites that half-words, bytes, and words are all processed by the aligning unit and the sign extension unit (Col.2 lines 36-46, 62-65 and Col.3 lines 1-16). As a result, Greenley and Dye both fail to disclose, teach, or suggest transferring a data value to a 'shifter circuit' in response to a determination that a pending instruction is a "load half-word operation" or a 'load-byte operation'. Greenley and Dye also both fail to disclose, teach or suggest transferring a data value to*

a 'target register' in response to a determination that a pending instruction is a 'load word operation'".

46. The Examiner disagrees with the Applicant's assertion that Greenley and Dye fail to teach "transferring a data value to a 'shifter circuit' in response to a determination that a pending instruction is a 'load half-word operation' or a 'load-byte operation'". Greenley has, in fact, taught such concepts, as was cited in the previous office action (see paragraphs 33-35 of the office action dated 11/18/03), and again in paragraphs 30-32 above. Greenley has taught that during a load half-word or load-byte operation, half-word or byte data values are transferred from the data cache to the alignment and sign extension units prior to be loaded into the target register (see Fig.1, Col.2 lines 8-47 and Col.5 lines 13-24 of Greenley).

47. Furthermore, as was cited in the previous office action (see paragraphs 33-35 of the office action dated 11/18/03), and again in paragraphs 30-32 above, Greenley in view of Dye has taught transferring a data value to a target register in response to a determination that a pending instruction is a load word operation. Here, Greenley shows a datapath that can transfer a "first data value" from a "data cache" to a "target register" via the sign extension and aligning units (see Fig.1 of Greenley, as well as above paragraphs 30-32). Greenley has not explicitly taught the bypassing of the sign extension unit (as shown in paragraph 31 above). The motivation to modify the datapath to bypass the sign extension unit comes from the Dye reference, which has taught bypassing portions of a circuit that are not needed in order to reduce the latency inherent in such circuitry (see Abstract and Col.3 lines 2-11, 35-43 of Dye). When data is fetched that occupies the entire register, no sign extension is necessary because of the lack of unoccupied bits, and thus sign extension and alignment units circuitry becomes unnecessary under these

circumstances (see above paragraphs 31-32). For example, Patterson et al., *Computer Organization & Design: The Hardware/Software Interface* has taught that attempting to sign extend a 32-bit word loaded into a 32-bit register is a moot operation as no unoccupied bits are available to sign extend (see p.214 of Patterson). Therefore, as stated above in paragraphs 30-32, one of ordinary skill in the art would have found it obvious to modify a processor to bypass circuitry that performs a moot operation so that latency in executing instructions that would have used said circuitry is reduced, and thus a data value can be transferred directly from the data cache to a target register without being processed by the sign extension and alignment units.

Conclusion

48. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

49. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the

patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

50. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

51. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
4/20/2004

Eddie Chan
EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100